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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/120,126	07/22/98	BAYS L	BAYS7-19-1-2

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EXAMINER	
MCLEAN, K	
ART UNIT	**PAPER NUMBER**
2185	11

DATE MAILED: 08/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/120,126	BAYS et al.
Examiner	**Art Unit**
Kimberly McLean	2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 12, 2001* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-8 and 10-23* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-8 and 10-23* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

1. The detailed enclosed action is in response to the Amendment submitted on June 12, 2001.

Claim Rejections - 35 U.S.C. § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Persaud (GBPN: 2074762) in view of Wu et al. (USPN: 5,659,715).

Regarding claims 13 and 16, Persaud discloses a first agent to provide a memory access clock signal to allow the first agent to access the shared memory and a second agent to provide a representation of the memory access clock signal to access the shared memory in synchronism with the access by the first agent to the shared memory (Page 1, Lines 39-65, Page 3, L 1-22). Persaud does not teach the use of an external non-dedicated memory nor the first and second agent accessing different portions of the shared memory simultaneous. Wu discloses an external non-dedicated memory which allows dynamic repartitioning/allocation between the agents thereby providing efficient usage of memory and flexibility (C 7, L 11-23). Additionally shared memory systems that support simultaneous access to different portions of the memory is well known in the

art. Simultaneous access improves the performance of the system by allowing a plurality of devices access to the memory without concurrent in oppose to always having to wait until another device is done accessing the memory. One of ordinary skill in the art would have recognized the benefits of Wu's teachings and the benefits of allowing simultaneous access and would have been motivated to use Wu's teachings along with using simultaneous access of a shared memory with Persaud's teachings for the desirable purpose of efficiency, flexibility and improved performance.

Regarding claim 15, Persaud does not explicitly disclose partitioning the shared memory into a first block such that the first agent has access to the a first partition and partitioning the shared memory block into a second partition such that the second agent has access to the second partition. However, this concept is known in the art for improving performance by providing simultaneous access to the memory. Therefore, it would have been obvious to one of ordinary skill in the art to partition the memory in Persaud's system for the desirable purpose of improved performance.

4. Claims 1-8, 10-12 and 20-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (USPN: 5,659,715) in view of Persaud (GBPN: 2074762).

Regarding claim 1, Wu discloses a system comprising an external non-dedicated memory (Figure 3, Reference 304; C 7, L 11-27); a first agent (system controller) adapted to access a first memory portion (C 4, L 58-65); and a second agent (graphics controller) adapted to access a second

memory portion (C 4, L 58-65); wherein the first portion and the second portion are variable (C 7, L 11-23). Wu does not explicitly disclose a first and second memory portion comprising a plurality of banks. However, it is common knowledge in the art for memory to comprise a plurality of banks or blocks. Such as system memory (DRAM, SDRAM etc.) in a computing system. Wu teaches the concept of dynamically allocating portions of memory to a first and second agent such that the performance of the memory is improved. One of ordinary skill in the art would have recognized the benefits of Wu's teachings and would have been motivated to use the teachings of Wu in a memory comprising a plurality of banks for the desirable purpose of flexibility and improved performance. Also, Wu does not disclose a second agent having a clock representation of a first agent's clock signal. However, Persaud teaches the concept of providing a master clock from a master processor (first agent) to slave processors (second agent) to synchronize the slaves'circuitry to the master clock to provide reliable and accurate data transfers between the master processor and the slave processor (Page 1, Lines 39-65, Page 3, L 1-22). One of ordinary skill in the art would have recognized the efficient use of memory provided by Wu's teachings and would have been motivated to use such teachings in a synchronous system using the features taught by Persaud for the desirable purpose of efficiency and improved performance.

Regarding claims 2-5, Wu discloses a register to set the number of banks (address space) accessible to the first and second agent (C 9, L 23-52).

Regarding claim 6, Wu discloses the limitations cited above in claim 1, however, Wu does not explicitly disclose a first and second agent as a digital signal processor. However, digital signal processors are known in the art for their use in high speed data manipulations used in audio, communications and other data acquisitions. Wu teachings provide an efficient way of dynamically allocating memory for two different functions. Clearly it would have been obvious to one of ordinary skill in the art to add a digital signal processor to the teachings of Wu for use in a system requiring high speed data manipulations for the desirable purpose of efficient memory usage.

Regarding claims 7-8 and 11, Wu discloses a plurality of agents (system controller and graphics controller)(C 4, L 58-65); an external non-dedicated shared asynchronous memory block accessible by each of the plurality of agents (C 7, L 1-65); a register adapted to partition the external non-dedicated shared memory block into a plurality of partitions, each plurality of partitions being accessible by a unique group of the plurality of agents (C 9, L 23-52). Wu does not explicitly disclose the shared memory block comprising a plurality of memory banks. However, it is common knowledge in the art for memory to comprise a plurality of banks or blocks. Such as system memory (DRAM, SDRAM etc.) in a computing system. Wu teaches the concept of dynamically allocating portions of memory to a first and second agent such that the performance of the memory is improved. One of ordinary skill in the art would have recognized the benefits of Wu's teachings and would have been motivated to use the teachings of Wu in a

memory comprising a plurality of banks for the desirable purpose of flexibility and improved performance. Additionally, Wu does not disclose a plurality of agents having a clock representation of a base clock signal. However, Persaud teaches the concept of providing a master clock (base clock) from a master processor (first agent) to slave processors (plurality of agents) to synchronize the slaves'circuitry to the master clock to provide reliable and accurate data transfers between the master processor and the slave processor (s) (Page 1, Lines 39-65, Page 3, L 1-22). One of ordinary skill in the art would have recognized the efficient use of memory provided by Wu's teachings and would have been motivated to use such teachings in a synchronous system using the features taught by Persaud for the desirable purpose of efficiency and improved performance.

Regarding claims 10 and 12, Wu discloses the limitations cited above in claim 1, however, Wu does not explicitly disclose a SDRAM . Synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Therefore it would have been obvious to one of ordinary skill in the art to use a SDRAM in Wu's system for increased speed and improved performance.

Regarding claims 20-21 and 23, Wu discloses a method comprising accessing a first portion of memory from a first agent (C 4, L 58-65); accessing a second portion of memory from a second agent (C 4, L 58-65); and repartitioning the shared memory on the fly (C 7, L 11-23). Wu does

not explicitly disclose accessing a plurality of banks from a first agent and accessing a second plurality of banks from a second agent. Wu teaches the concept of allocating portions of memory to a first and second agent. It is well known in the art that to partition memory into blocks, pages or banks and it would have been obvious to one of ordinary skill in the art to use the teachings of Wu in a memory comprising a first and second plurality of banks for the desirable purpose of flexibility and improved performance. Also, Wu does not disclose a second agent having a clock representation of a first agent's clock signal. However, Persaud teaches the concept of providing a master clock from a master processor (first agent) to slave processors (second agent) to synchronize the slaves'circuitry to the master clock to provide reliable and accurate data transfers between the master processor and the slave processor (Page 1, Lines 39-65, Page 3, L 1-22). One of ordinary skill in the art would have recognized the efficient use of memory provided by Wu's teachings and would have been motivated to use such teachings in a synchronous system using the features taught by Persaud for the desirable purpose of efficiency and improved performance.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable in view of Persaud (GBPN: 2074762) and Wu (USPN: 5659715) as applied to claim 13 above and further in view of Hughes (USPN: 5,784,582).

Regarding claims 14, Persaud discloses the features stated above in claim 13, however, Persaud does not explicitly disclose the shared memory servicing the first and second agent without a wait

state in between. Hughes does teach this feature (C 3, L 14-21; C 6, L 39-57; C 7). This feature taught by Hughes improves system bandwidth, thereby, improving the performance of the system. Therefore it would have been obvious to one of ordinary skill in the art to use the teachings of Hughes in the system taught by Persaud and Wu for the desirable purpose of improved performance.

6. Claims 17-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Persaud (GBPN: 2074762) in view of Wu (USPN: 5,659,715) and Hughes (USPN: 5,784,582). Regarding claims 17-19 and 22, Persaud discloses providing a memory access clock signal by the first agent (BUS 02 clock signal; Page 5, L 1-10); providing a representation of the memory access clock signal in synchronism with the memory access clock signal (clock signal 02, Page 5, L 21-28); regenerating in the second agent the memory access clock signal (Page 5, L 21-28); firstly accessing the shared memory from a first agent (master processor) based on the memory access clock signal (Page 1, L 39-65; Page 9-10 with respect to Figure 11); secondly accessing the shared memory from a second agent based on the representation (regenerated) memory access clock signal (Page 1, L 39-65; Page 9-10 with respect to Figure 11). Persaud does not explicitly disclose secondly accessing the shared memory following the step of firstly accessing without a wait state therebetween and Persaud does not teach the use of an external non-dedicated memory nor the first and second agent accessing portions of the shared memory. Wu discloses an external non-dedicated memory which allows dynamic repartitioning/allocation between the agents thereby

providing efficient usage of memory and flexibility (C 7, L 11-23). Hughes teaches secondly accessing a shared memory following the step of firstly accessing the shared memory without a wait state therebetween (C 3, L 14-21; C 6, L 39-57; C 7). This feature taught by Hughes improves system bandwidth, thereby, improving the performance of the system. Additionally shared memory systems that support access to portions of the memory is well known in the art, particularly with systems that support simultaneous access to the shared memory. Simultaneous access improves the performance of the system by allowing a device access to the memory even if another device is accessing the memory in oppose to having to wait until another device is done accessing the memory.. Therefore it would have been obvious to one of ordinary skill in the art to use the teachings of Hughes along with accessing portions of the shared memory (for simultaneous access) in the system taught by Persaud for the desirable purpose of improved performance.

Response to Arguments

7. Applicant's arguments with respect to claim have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly McLean whose telephone number is (703) 308-9592 (e-mail address: Kimberly.McLean2@uspto.gov). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9000.

Any formal response to this action intended for entry should be mailed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to (703) 305-9051 and labeled "FORMAL" or "OFFICIAL". Any informal or draft communication should be faxed to (703) 305-9731 and labeled "INFORMAL" or "UNOFFICIAL" or "DRAFT" or "PROPOSED" and

followed by a phone call to the Examiner at the above number. Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

KNM

KNM

August 17, 2001

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
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